## **ABSTRACT**

Please delete the Abstract and replace it with the following:

A method for determining an interconnect delay at a node in an interconnect having a plurality of nodes. The method includes performing a bottom-up tree traversal to compute the first three admittance moments for each of the nodes in the interconnect. The computed admittance moments are utilized, in an advantageous embodiment, to compute a pi-model of the downstream load. Next, the equivalent effective capacitance value  $C_{\rm eff}$  is computed utilizing the components of the computed pi-model and the Elmore delay at the node under evaluation. In an advantageous embodiment,  $C_{\rm eff}$  is characterized by:

$$C_{\text{eff}} = C_{\text{fi}}(1 - e^{-T/\tau dj})$$

where  $C_{ij}$  is the far-end capacitance of the pi-model at the node, T is the Elmore delay at the node and  $\tau dj$  is the resistance of the pi-model ( $R_{dj}$ ) multiplied by  $C_{ij}$ . The interconnect delay at the node is then determined utilizing an effective capacitance metric (ECM) delay model.